



PLL Design Capability ...

High performance timing PLL's are a critical element to the success of System on Chip (SoC) designs. Without a reliable low jitter clock source today's high performance devices will be ineffective. By working with Moortec's highly experienced timing design team we will help you to reduce this risk and achieve improved time to revenue.

We have a long history of providing reliable, accurate and easy to integrate PLL IP blocks to enable seamless SOC design.



.... for System on Chip

Capabilities Include:

High Performance PLL Design

- High supply noise immunity
- 65nm, 0.13um, 0.18um, 0.35um designs
- Low power <14mW
- Low phase Jitter <1ps
- Integrated loop filter
- Programmable loop bandwidth
- Power down
- Designed to operate in a digital environment

Design Examples

- Temperature Sensors
- ADCs & DACs
- VCOs & Crystal oscillators
- Power management
- ESD & I/O Cells
- Low noise amplifiers
- CMOS Band Gap voltage reference
- Power on reset

You choose...



Moortec - the perfect partner to provide high performance analog / mixed signal IP and support for your SoC and Digital ASIC designs

tel +44 (0)1752 693800

email info@moortec.com

web www.moortec.com