



Silicon IP Design ...

High performance Analog and Mixed Signal IP, such as PLLs, ADCs, DACs, I/O cells and ESD structures, are a critical element to the success of System on Chip (SoC) designs. By working with Moortec's highly experienced design team we will help you to reduce IC design risk and time to revenue.

We pride ourselves on our flexibility, and will provide IP blocks for integration or provide a complete chip - along with IC support for test/load boards, evaluation kits and reference designs - to smooth your path to market.



.... for System on Chip

Capabilities Include:

Analog IP Design

- Transistor level analog/RF IC design (BiCMOS, CMOS 0.6um to 65nm)
- Full custom IC layout
- Ultra low power sub-threshold design techniques
- Chip level design methodologies (ESD, supplies, substrate noise, floor planning)

Design Examples

- Low jitter PLLs (<1ps rms jitter)
- Flexible, low power PLLs
- VCOs & Crystal oscillators
- Power management
- ESD & I/O Cells
- Low noise amplifiers
- CMOS Band Gap voltage reference

You choose...



Moortec - the perfect partner to provide high performance analog / mixed signal IP and support for your SoC and Digital ASIC designs

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