



Description

MR74045 – Flexible High Performance PLL
 0.13um CMOS General Purpose Phase Locked Loop
 Clock Generation, Multiplication & Skew Control

Part Number:

Features:

- High performance
- Very High Supply Noise Immunity
- Low Phase Offset (<100ps)
- Low Phase Jitter (down to 8ps)
- Very Low Cycle-Cycle & Period Jitter
- Low power consumption (max 14mW)

Technology:

TSMC 0.13um Logic
 1P6M Salicide CU
 FSG 1.2V, 3.3V CMOS

Deliverables:

- GDSII
- Abstract
- Design Report
- Verilog- A Models
- Verilog Models

Circuit Status:

Silicon proven

Design rights:

Customer owned.

Overview:

Optimised for high supply immunity and low phase (interval) jitter.

- Input clock frequencies from 3.2MHz to 160MHz
- Output clock frequencies from 40MHz to 640MHz
- High performance
- Very High Supply Noise Immunity
- Low Phase Jitter (7.6ps rms Fout=640MHz)
- Low Cycle-Cycle & Period Jitter (20ps)
- Low Phase Offset (<100ps)
- Low power consumption (max 14mW)
- Good Output Duty Cycle (45%-55% at 320-640MHz and 49%-51% at 40-320MHz)
- Feedback Input for Skew Control
- Internal programmable divider for clock multiplication (1-128)
- Integrated Programmable Loop Filter
- Programmable Loop Bandwidth (160kHz – 1280kHz) for jitter optimisation
- Settling Time (300us max)
- Supply 2.5v (1.2v as reference)
- Power Down
- Test
- Integrated test methodology including VCO and CHP tests
- Full power down
- Compatible with Iddq testing
- Clock bypass mode for chip testing & simulation

Symbol View:

