



Description

MR74032 – Flexible High Performance PLL
 65nm CMOS General Purpose Phase Locked Loop
 Clock Generation, Multiplication & Skew Control

Part Number:
 MR74032

Features:

- High performance
- Very High Supply Noise Immunity
- Low Phase Offset (<100ps)
- Low Phase Jitter (down to 8ps)
- Very Low Cycle-Cycle & Period Jitter
- Low power consumption (max 14mW)

Technology:
 TSMC 65nm LP 1.2V, 2.5V Standard CMOS 1P5M

Deliverables:

- GDSII
- Abstract
- Design Report
- Verilog- A Models
- Verilog Models

Circuit Status:
 Silicon proven

Design rights:
 Customer owned.

Overview:

Optimised for high supply immunity and low phase (interval) jitter.

- Input clock frequencies from 4MHz to 160MHz
- Output clock frequencies from 50MHz to 800MHz
- High performance
- Very High Supply Noise Immunity (VCO $\Delta F < 0.1\%$ at 100mv at DC-1GHz)
- Low Phase Jitter (8 to 16ps rms or 0.02% Input Period rms)
- Very Low Cycle-Cycle & Period Jitter (20ps)
- Low Phase Offset (<100ps)
- Low power consumption (max 14mW)
- Cell area 0.2mm² (379.7um x 521.4um)
- Good Output Duty Cycle (45%-55% at 400-800MHz and 48%-52% at 50-400MHz)
- Feedback Input for Skew Control
- Internal programmable divider for clock multiplication (1-128)
- Integrated Programmable Loop Filter
- Programmable Loop Bandwidth (200kHz – 1800kHz) for jitter optimisation
- Settling Time (<200us)
- Supply 2.5v (1.2v as reference)
- Power Down
- Lock Detector
- Test
- Integrated test methodology including VCO and CHP tests
- Full power down
- Compatible with Iddq testing
- Clock bypass mode for chip testing & simulation

Symbol View:

